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THE DESIGN OF COMPUTATIONAL UNIT FOR HIGH SPEED RECONFIGURABLE PROCESSORS

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Abstract

Reconfigurable computing is intended to fill the gap between hardware and software by providing an ideal platform for scientific and commercial computations. The platform tends to be as much flexible as that of General Purpose Processors (GPP) and also tends to be as much high speed as that of Application Specific Integrated Circuits (ASICs). Reconfigurable processors are one of the most advanced solutions being proposed for reconfigurable computing. The performance of Reconfigurable processor is greatly dependent on the design of its reconfigurable computational unit. A large number of designs for such kind of computational units have already been proposed but majority of them are suffering from the problem of enormous configuration overheads. In this research paper, a high speed computational unit design for reconfigurable processors has been proposed. The proposed design is using many emerging techniques like multi port configuration memory, intelligent configuration updating, concurrent configuration mapping and multi-threaded configuration controller. The proposed design has been stimulated for the execution of a variety of different application programs. The performance statistics are at an excellent level for the design of the high speed reconfigurable processors with the tendency of minimum possible configuration overheads. Thus, it can be used to enhance the performance of high speed scientific and commercial applications.

Keywords : GPPs, ASICS, FPGAs, RFUs, Reconfigurable computing, Configurable processors, RFU coupling